AMENDMENTS TO THE SPECIFICATION

1. Please replace paragraph [0005] with the following amended paragraph:

[0005] Please refer to Fig.1 and Fig.2. Fig.1 is a schematic diagram of a prior art TFT-LCD. Fig.2 is an equivalent circuit diagram of the TFT-LCD. The TFT-LCD 10 comprises a lower substrate 12. The lower substrate 12 comprises a pixel array 14, a scanning line driving circuit 16, and a data line driving circuit 18. The pixel array 14 includes a plurality of scanning lines (not shown) and a plurality of data lines (not shown). A plurality of pixels (ex. pixels A, B, C, [[B"]]B', and [[C"]]C') is therefore defined by the scanning lines and the data lines. The pixel A, B, and C are located on the same scanning line, while the pixel A, [[B"]]B' and [[C"]]C' are located on the same data line.

2. Please replace paragraph [0009] with the following amended paragraph:

[0009] ~~$V_{FD}=[C_{GS}/(C_{LC}+C_{SC}+C_{GS})]*\Delta VG$ (1)~~

$V_{FD}=[C_{GS}/(C_{LC}+C_{SC}+C_{GS})]*\Delta V_G$ (1)

3. Please replace paragraph [0012] with the following amended paragraph:

[0012] Furthermore, the resistances of the bus lines are so large that as a pulse voltage is

input into the driver IC chips from the bus lines 17, the input voltages of the driver IC chips are different from one another, which leads to different waveforms of output voltages output from the driver IC chips. For example, as shown in Fig.3, the waveforms of the output voltages output from the chips 16a, 16b, and 16c are quite different. The voltage difference (ΔV_{GA}) output from the chip 16a is larger than the voltage difference [[(ΔVGB)]] ($\Delta V_{GB'}$) output from the chip 16b, which is larger than the voltage difference [[(ΔVGC)]] ($\Delta V_{GC'}$) output from the chip 16c. Therefore, a feed-through voltage of a pixel will decrease as the distance between the data line driving circuit and the pixel increases. That is, as shown in Fig.1, feed-through voltage of the pixel A is larger than that of the pixel [[B"]] B', whose feed-through voltage is larger than that of the pixel [[C"]] C' (that is, ~~$(V_{FD})_A > (V_{FD})_B > (V_{FD})_C$~~ $(V_{FD})_A \geq (V_{FD})_{B'} \geq (V_{FD})_{C'}$), which make flicker that reduces display quality of an LCD panel.

4. Please replace paragraph [0048] with the following amended paragraph:

[0048] Please refer to Fig.8. Fig.8 is a top view of a pixel array of an LCD panel according to the fourth embodiment of the present invention. Moreover, the fourth embodiment of the present invention is implemented

according the above-mentioned method (1). As shown in Fig.8, a pixel array 80 comprises at least a plurality of scanning lines 82a and 82b electrically connected to a scanning line driving circuit 84, and data lines 86a, 86b electrically connected to a data line driving circuit 88. Additionally, the pixel array 80 further comprises pixels A, [[B"]] B', and [[C"]] C', which correspond to the pixels A, [[B"]] B', and [[C"]] C' of Fig.1. The pixels A, [[B"]] B', and [[C"]] C' comprise thin film transistors T_A, [[TB]] $T_{B'}$, [[TC]] $T_{C'}$ and corresponding liquid crystal cells (not shown). The gate electrodes 92a, 92b, 92c of thin film transistors T_A, [[TB]] $T_{B'}$, [[TC]] $T_{C'}$ are connected to the scanning lines 82a. The drain electrodes 94a, 94b, 94c of the thin film transistors T_A, [[TB]] $T_{B'}$, [[TC]] $T_{C'}$ are respectively connected to the data line 86a. The source electrodes 96a, 96b, 96c of thin film transistors T_A, [[TB]] $T_{B'}$, [[TC]] $T_{C'}$ are connected to pixel electrodes 90a, 90b, 90c of the liquid crystal cells respectively. Furthermore, semi-conductive layers 98a, 98b, 98c are separately disposed between the gate electrodes and the source, the drain electrodes.

5. Please replace paragraph [0049] with the following amended paragraph:

[0049] In addition, as shown in Fig.8, the pixel

electrodes 90a, 90b, and 90c include extension portions 99a, 99b, and 99c. Thus, overlapping region 100a, 100b, and 100c are formed in the pixels A, [[B"]] B', and[[C"]] C'. The overlapping region 100a is formed by lapping the extension portion 99a over the scanning line 82a. Similarly, the overlapping regions 100b, 100c are respectively formed by lapping the extension portions 99b, 99c over the scanning lines 82a. The area of the overlapping region 100a is smaller than that of the overlapping region 100b, whose area is smaller than that of the overlapping region 100c. Additionally, the pixel electrodes 90a, 90b, and 90c are lapped over the scanning lines 82b to form overlapping regions 102a, 102b, and 102c, which form the storage capacitors of the pixels A, [[B"]] B', and [[C"]] C'.

6. Please replace paragraph [0050] with the following amended paragraph:

[0050] In the fourth embodiment, the overlapping regions 100a, 100b, and 100c respectively correspond to the compensating capacitors C_A, [[CB]] $C_{B'}$, and [[CC]] $C_{C'}$ (not shown). Since the areas of the overlapping regions 100a, 100b, and 100c are increased sequentially, the capacitance of the compensating capacitor C_A is smaller than the capacitance of the compensating capacitor [[CB]] $C_{B'}$, whose

capacitance is smaller than that of the compensating capacitor [[CC]] $C_{C'}$ (i.e. ~~$C_A<C_B<C_C$~~ $C_A<C_{B'}<C_{C'}$). Thus, feed-through voltages of pixels A, [[B"]] B', [[C"]] C', are approximately equal (that is, ~~$(V_{FD})_A \approx (V_{FD})_B \approx (V_{FD})_C$~~ $(V_{FD})_A \approx (V_{FD})_{B'} \approx (V_{FD})_{C'}$).